

# M-4

## HIGH-POWER AND HIGH-EFFICIENCY ION-IMPLANTED POWER GaAs FETs FOR C AND X BANDS

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### ABSTRACT

C- and X-band multichip operation power GaAs FETs have been developed using an ion implantation technique. Uniformity among chips superior to and breakdown voltage comparable to those of conventional GaAs FETs have been obtained. The 4-chip C-band device, with a total gate width ( $W_g$ ) of 57.6 mm, delivers a CW output power at 1-dB gain compression ( $P_{1dB}$ ) of 21 W with 9 dB gain (G) and 42 % power-added efficiency ( $\eta_{add}$ ), and a saturated output power ( $P_{sat}$ ) of 25 W at 5 GHz. The 8-chip X-band device with  $W_g$ =32 mm gives  $P_{1dB}$ =10.5 W with G=5 dB and  $\eta_{add}$ =25 %, and  $P_{sat}$ =12 W at 10 GHz. The channel temperature rise is estimated from IR measurement to be 40 °C and 47 °C at 21-W and 10.5-W output power for the C- and X-band devices, respectively.

### INTRODUCTION

Multichip operation is indispensable for realizing high-power GaAs FETs. In view of power-combining efficiency, good uniformity among chips is a prerequisite for multichip operation to be feasible. Most of the power GaAs FETs reported to date have been fabricated using epitaxial wafers grown by Ga/AsCl<sub>3</sub>/H<sub>2</sub> vapor phase epitaxy (VPE) (1)(2) or metal-organic chemical vapor deposition (MOCVD) (3). On the other hand, ion implantation provides a potentially superior means of preparing uniform wafers.

To the authors' knowledge, relatively few papers have been published on ion-implanted power GaAs FETs. Feng et al.(4) and Doerbeck et al.(5) reported on ion-implanted GaAs FETs with an output power of 1.6-2.2 W at 10 GHz.

The purpose of this paper is to report on multichip operated C- and X-band power GaAs FETs fabricated by direct ion implantation into semi-insulating GaAs wafers. The FETs deliver 10-20 W output power with 25-42 % power-added efficiency at X and C bands, which is the state-of-the-art performance of the ion-implanted FETs.

### DEVICE FABRICATION

The starting wafers are undoped LEC semi-insulating GaAs substrates with 2-inch diameter and (100) orientation. The n-type channel layer is formed by selective double implantation of Si<sup>+</sup> ions, first at 50 keV with a dose of  $1.0 \times 10^{12} \text{ cm}^{-2}$  and then at 200 keV with a dose of  $3.3 \times 10^{12} \text{ cm}^{-2}$ . Next, ion implantations with a dose of  $2 \times 10^{18} \text{ cm}^{-2}$  are performed successively at 50, 120 and 250 keV to form r layers for source and drain. The implanted wafers are capless-annealed at 850 °C for 15 minutes in pure argon ambient containing a small amount of arsine (AsH<sub>3</sub>). The peak carrier concentration of channel layer is  $1.2 \times 10^{17} \text{ cm}^{-3}$  measured by C-V method. The source and drain ohmic contacts are formed by alloying Pt/AuGe. Aluminum is used for the gate electrode. The gate length and unit gate width are 1.3 μm and 200 μm for C-band devices, and 0.7 μm and 100 μm for X-band devices. The cross section of the devices is schematically shown in Fig. 1. For the C-band devices, two kinds of chips with total gate width ( $W_g$ ) of 7.2 mm and 14.4 mm have been fabricated. Fig. 2 shows the top views of these chips. The X-band chip, shown in Fig. 3, has  $W_g$ =4 mm. The chips do not have plated heat sink, via hole and air bridge.

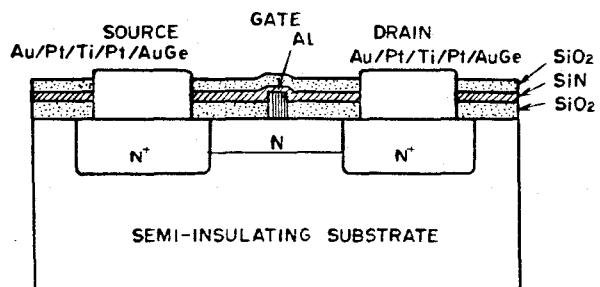
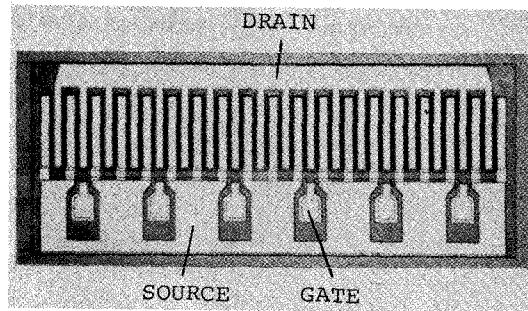
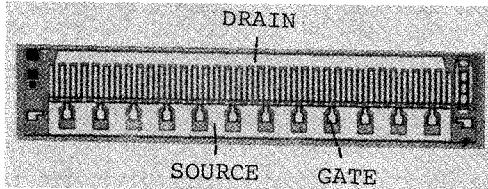


Fig. 1. Schematic cross section of ion-implanted power GaAs FET (unit cell)

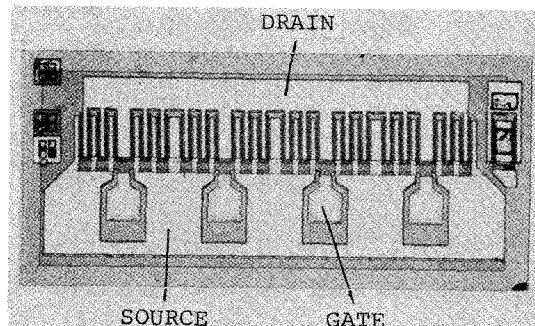


(a)  $W_g = 7.2 \text{ mm}$ , chip size =  $1.4 \text{ mm} \times 0.6 \text{ mm}$



(b)  $W_g = 14.4 \text{ mm}$ , chip size =  $2.9 \text{ mm} \times 0.6 \text{ mm}$

Fig. 2. Top view of C-band power GaAs FET chips



$W_g = 4 \text{ mm}$ , chip size =  $1.2 \text{ mm} \times 0.6 \text{ mm}$

Fig. 3. Top view of X-band power GaAs FET chip

#### C-BAND DEVICE

Saturated drain current ( $I_{DSS}$ ) has been measured on about 80 samples of the 7.2 mm chip randomly picked up across a 2-inch ( $20 \text{ cm}^2$ ) wafer. The distribution of  $I_{DSS}$  is shown in Fig. 4, in comparison with that of the FETs fabricated on a  $6 \text{ cm}^2$  MOCVD wafer. Standard deviation ( $\sigma$ ) of ion-implanted FETs has been found to be 4.1 % of the average  $I_{DSS}$  ( $\bar{I}_{DSS}$ ) of 1.6 A, in contrast to 7.7 % of the FETs with  $\bar{I}_{DSS} = 1.5 \text{ A}$  fabricated on a MOCVD wafer.

The source-drain breakdown voltage of the implanted FETs has been measured at  $1/2 \bar{I}_{DSS}$  under pulsed conditions of  $0.1 \mu\text{s}$  pulse width and 0.1 % duty factor. It has been found to be more than 40 V, which is comparable to that of our epitaxial devices and high enough to be

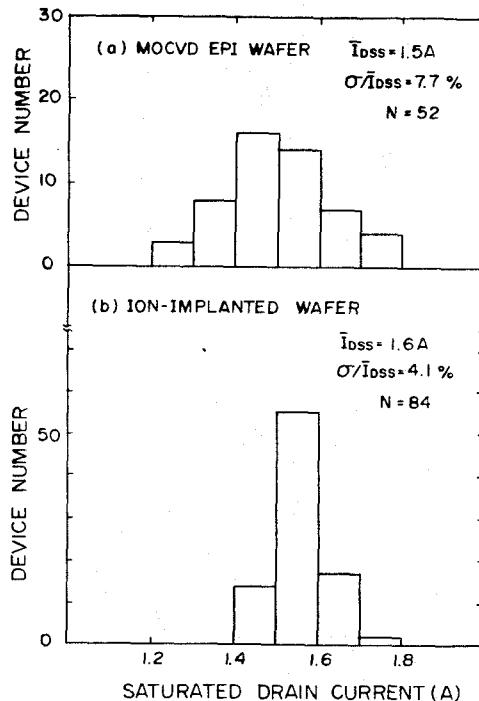
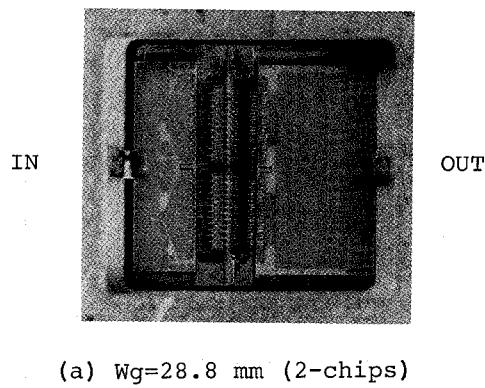


Fig. 4.  $I_{DSS}$  distribution of C-band FETs with  $W_g = 7.2 \text{ mm}$  prepared by (a) MOCVD and (b) ion implantation

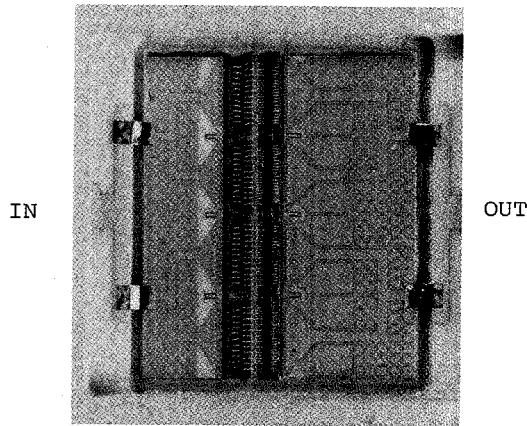
operated at a drain-source voltage of 10 V.

One-chip devices with  $W_g = 7.2 \text{ mm}$  and  $14.4 \text{ mm}$ , 2-chip device with  $W_g = 28.8 \text{ mm}$  ( $14.4 \text{ mm} \times 2$ ), and 4-chip device with  $W_g = 57.6 \text{ mm}$  ( $14.4 \text{ mm} \times 4$ ) have been assembled in ceramic packages. The devices other than the 7.2-mm device are internally matched at both input and output ports using lumped and distributed elements. The internal views of the 2- and 4-chip devices are shown in Fig. 5.

The rf performance of these devices at 5 GHz under drain-source voltage ( $V_{DS}$ ) of 10 V is shown in Fig. 6. Output powers at 1-dB gain compression ( $P_{1dB}$ ) of 33.5, 36.7, 40.5 and 43.2 dBm with gains ( $G$ ) of 10.5, 10.2, 10.5 and 9 dB and power-added efficiencies ( $\eta_{add}$ ) of 36, 37, 40 and 42 % have been obtained from 7.2-, 14.4-, 28.8- and 57.6-mm devices, respectively. Saturated output power of 25 W has been delivered from the 57.6 mm device. It is to be noted that the power-combining efficiency ( $\eta_c$ ) is nearly 100 % up to the 4-chip device with  $W_g = 14.4 \text{ mm} \times 4$  as can be seen from Fig. 7. A typical output power versus frequency characteristic for the 57.6-mm device is shown in Fig. 8, where the input power ( $P_{in}$ ) is kept at 37 dBm. More than 20 W (43 dBm) of output power is obtained over 4.8 to 5.25 GHz. Fig. 9 shows an output power distribution of the 28.8-mm device, measured at 5 GHz



(a)  $W_g = 28.8$  mm (2-chips)



(b)  $W_g = 57.6$  mm (4-chips)

Fig. 5. Internally matched C-band power GaAs FETs

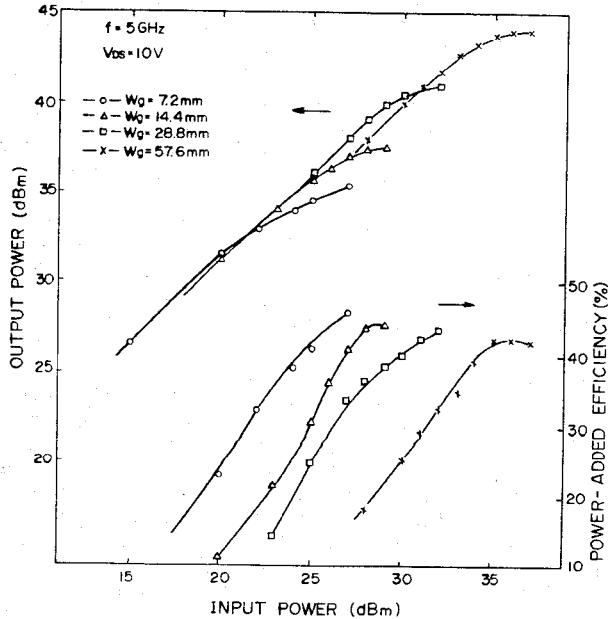


Fig. 6. Output power and power-added efficiency versus input power at 5 GHz for C-band FETs with  $W_g = 7.2$  mm, 14.4 mm, 28.8 mm and 57.6 mm

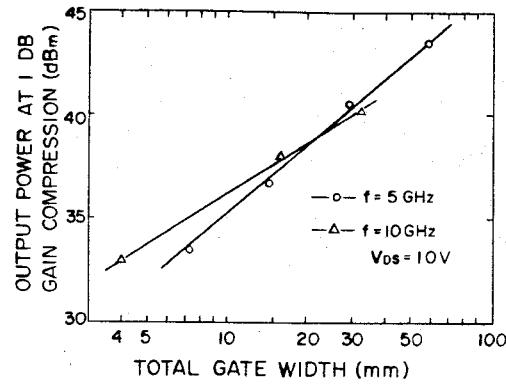


Fig. 7. Output power at 1-dB gain compression versus total gate width ( $W_g$ ) for C- and X-band FETs

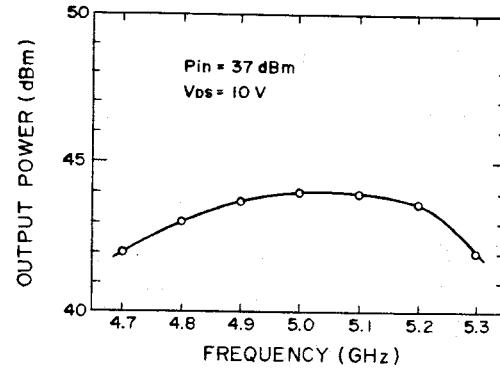


Fig. 8. Output power versus frequency for the 57.6 mm device

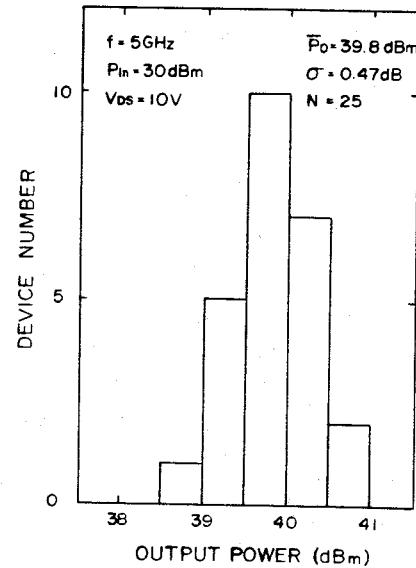


Fig. 9. Output power distribution of C-band FETs with  $W_g = 28.8$  mm (2-chips) at 5 GHz for input power of 30 dBm

for  $P_{in}=30$  dBm using a test fixture that consists of only 50-ohm input and output microstrip lines. The standard deviation ( $\sigma$ ) is a very small value of 0.47 dB, indicating that the ion-implanted FETs are also uniform rf-wise as well as dc-wise. A typical thermal resistance has been found to be 1.4 °C/W for the 57.6-mm device from IR scanning microscope measurement. The channel temperature rise,  $\Delta T_{ch}$ , is estimated to be about 40 °C when the device delivers 21-W output power at 5 GHz.

#### X-BAND DEVICE

The rf measurements of X-band devices have been performed at 10 GHz on 1-chip devices with  $W_g=4$  mm (Fig. 3), 4-chip devices with  $W_g=16$  mm and 8-chip devices with  $W_g=32$  mm, assembled in ceramic packages. The measured results are shown in Fig. 10. The 4- and 8-chip devices are internally matched at both input and output ports.  $P_{1dB}$  of 33.0, 38.0 and 40.2 dBm with  $G$  of 6.3, 5.7 and 5.0 dB and  $\eta_{add}$  of 38, 37 and 25 % have been obtained for the 1-, 4- and 8-chip devices, respectively. Saturated output power of 12 W has been delivered from the 32-mm device. Power-combining efficiency of 80 % has been achieved up to 8-chips ( $W_g=32$  mm) as can be seen from Fig. 7. The efficiency degradation relative to that of C-band devices may be partly due to the insufficient internal matching circuitry. The

measures of improvement is being undertaken. A typical thermal resistance has been measured to be 2.2 °C/W for the 32-mm device, and  $\Delta T_{ch}$  is estimated to be 47 °C when the device delivers 10.5-W output power.

#### CONCLUSION

Ion-implanted power GaAs FETs have been developed that deliver  $P_{1dB}=21$  W with  $G=9$  dB and  $\eta_{add}=42$  % and  $P_{sat}=25$  W at 5 GHz, and  $P_{1dB}=10.5$  W with  $G=5$  dB and  $\eta_{add}=25$  % and  $P_{sat}=12$  W at 10 GHz. The 57.6-mm C-band device gives more than 20 W output power over 4.8 to 5.25 GHz. These output power levels are the highest ones reported so far on ion-implanted power GaAs FETs.

The source-drain breakdown voltage is more than 40 V. The thermal resistance (the channel temperature rise) are 1.4 °C/W (40 °C) and 2.2 °C/W (47 °C) for the 57.6-mm C-band device and the 32-mm X-band device, respectively, ensuring a reliable operation of these high-power devices.

20-W power GaAs FETs for upper C-band frequencies (6-8 GHz) are presently under development. X-band power GaAs FETs are also being improved in terms of power-combining efficiency and power gain.

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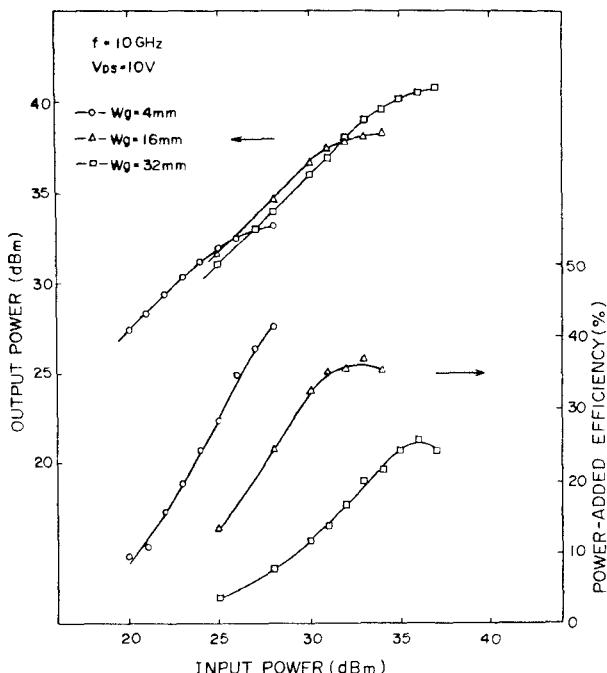


Fig.10. Output power and power-added efficiency versus input power at 10 GHz for X-band FETs with  $W_g=4$  mm, 16mm and 32 mm